14-Bit, 40 MSPS/65 MSPS A/D Converter

AD6644

FEATURES
- 65 MSPS Guaranteed Sample Rate
- 40 MSPS Version Available
- Sampling Jitter < 300 fs
- 100 dB Multitone SFDR
- 1.3 W Power Dissipation
- Differential Analog Inputs
- Digital Outputs
  - Twos Complement Format
  - 3.3 V CMOS Compatible
  - Data Ready for Output Latching

APPLICATIONS
- Multichannel, Multimode Receivers
- AMPS, IS-136, CDMA, GSM, Third Generation
- Single Channel Digital Receivers
- Antenna Array Processing
- Communications Instrumentation
- Radar, Infrared Imaging
- Instrumentation

PRODUCT DESCRIPTION

The AD6644 is a high speed, high performance, monolithic 14-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on-chip to provide a complete conversion solution. The AD6644 provides CMOS compatible digital outputs. It is the third generation in a wideband ADC family, preceded by the AD9042 (12-bit 41 MSPS) and the AD6640 (12-bit 65 MSPS, IF sampling).

Designed for multichannel, multimode receivers, the AD6644 is part of ADI's new SoftCell™ transceiver chipset. The AD6644 achieves 100 dB multitone, spurious-free dynamic range (SFDR) through the Nyquist band. This breakthrough performance eases the burden placed on multimode digital receivers (software radios) which are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio is 74 dB.

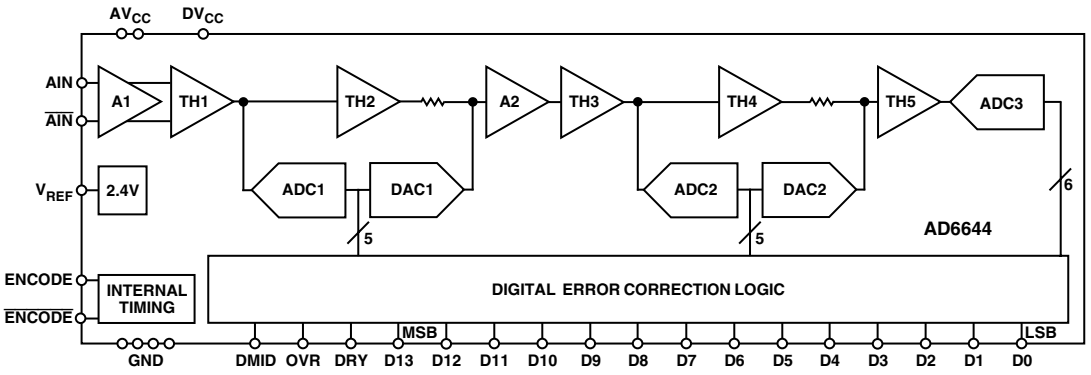
The AD6644 is also useful in single channel digital receivers designed for use in wide-channel bandwidth systems (CDMA, W-CDMA). With oversampling, harmonics can be placed outside the analysis bandwidth. Oversampling also facilitates the use of decimation receivers (such as the AD6620), allowing the noise floor in the analysis bandwidth to be reduced. By replacing traditional analog filters with predictable digital components, modern receivers can be built using fewer RF components, resulting in decreased manufacturing costs, higher manufacturing yields, and improved reliability.

The AD6644 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative, multipass circuit architecture. Units are packaged in a 52-lead Plastic Low Profile Quad Flat Pack (LQFP) specified from –25°C to +85°C.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 65 MSPS.
2. Fully differential analog input stage.
3. Digital outputs may be run on 3.3 V supply for easy interface to digital ASICs.
4. Complete solution: reference and track-and-hold.
5. Packaged in small, surface-mount, plastic, 52-lead LQFP.

FUNCTIONAL BLOCK DIAGRAM



REV. C

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AD6644–SPECIFICATIONS

DC SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} = –25°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Unit
RESOLUTION				14			14		Bits
ACCURACY									
No Missing Codes	Full	II		Guaranteed			Guaranteed		
Offset Error	Full	II	–10	3	+10	–10	3	+10	mV
Gain Error	Full	II	–10	– 6	+10	–10	–6	+10	% FS
Differential Nonlinearity (DNL)	Full	II	–1.0	±0.25	+1.5	–1.0	±0.25	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		±0.50			±0.50		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		10			10		ppm/°C
Gain Error	Full	V		95			95		ppm/°C
POWER SUPPLY REJECTION (PSRR)	Full	V		±1.0			±1.0		mV/V
REFERENCE OUT (V_{REF})	Full	V		2.4			2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Differential Input Voltage Range	Full	V		2.2			2.2		V p-p
Differential Input Resistance	Full	V		1			1		kΩ
Differential Input Capacitance	25°C	V		1.5			1.5		pF
POWER SUPPLY									
Supply Voltage									
AV_{CC}[1]	Full	II	4.85	5.0	5.25	4.85	5.0	5.25	V
DV_{CC}	Full	II	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Current									
IA_{VCC} (AV_{CC} = 5.0 V)	Full	II		245	276		245	276	mA
ID_{VCC} (DV_{CC} = 3.3 V)	Full	II		30	36		30	36	mA
Rise Time[2]									
AV_{CC}	Full	IV						15	ms
POWER CONSUMPTION	Full	II		1.3	1.5		1.3	1.5	W

NOTES
[1]AV_{CC} may be varied from 4.85 V to 5.25 V. However, rated ac (harmonics) performance is valid only over the range AV_{CC} = 5.0 V to 5.25 V.
[2]Specified for dc supplies with linear rise time characteristics.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} = –25°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Unit
ENCODE INPUTS (ENC, $\overline{ENC}$)									
Differential Input Voltage[1]	Full	IV	0.4			0.4			V p-p
Differential Input Resistance	25°C	V		10			10		kΩ
Differential Input Capacitance	25°C	V		2.5			2.5		pF
LOGIC OUTPUTS (D13–D0, DRY, OVR)									
Logic Compatibility				CMOS			CMOS		
Logic "1" Voltage[2]	Full	V		2.5			2.5		V
Logic "0" Voltage[2]	Full	V		0.4			0.4		V
Output Coding				Twos Complement			Twos Complement		
DMID	Full	V		DV_{CC}/2			DV_{CC}/2		V

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially. Reference TPC 15 for performance versus encode power.
[2]Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF will degrade performance.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{ENCODE}$ = Maximum Conversion Rate MSPS; T_{MIN} = –25°C, T_{MAX} = +85°C)

Parameter	Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Unit
Maximum Conversion Rate	Full	II	40			65			MSPS
Minimum Conversion Rate	Full	IV			15			15	MSPS
ENCODE Pulsewidth High	Full	IV	10			6.5			ns
ENCODE Pulsewidth Low	Full	IV	10			6.5			ns

Specifications subject to change without notice.

AC SPECIFICATIONS[1] (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{ENCODE}$ = Maximum Conversion Rate MSPS; T_{MIN} = –25°C, T_{MAX} = +85°C)

Parameter		Temp	Test Level	AD6644AST-40 Min	AD6644AST-40 Typ	AD6644AST-40 Max	AD6644AST-65 Min	AD6644AST-65 Typ	AD6644AST-65 Max	Unit
SNR										
Analog Input	2.2 MHz	25°C	II		74.5		72	74.5		dB
@ –1 dBFS	15.5 MHz	25°C	II		74.0		72	74.0		dB
	30.5 MHz	25°C	II		73.5		72	73.5		dB
SINAD[2]										
Analog Input	2.2 MHz	25°C	II		74.5		72	74.5		dB
@ –1 dBFS	15.5 MHz	25°C	II		74.0		72	74.0		dB
	30.5 MHz	25°C	V		73.0			73.0		dB
WORST HARMONIC (2^{ND} or 3^{RD})[2]										
Analog Input	2.2 MHz	25°C	II		92		83	92		dBc
@ –1 dBFS	15.5 MHz	25°C	II		90		83	90		dBc
	30.5 MHz	25°C	V		85			85		dBc
WORST HARMONIC (4^{TH} or Higher)[2]										
Analog Input	2.2 MHz	25°C	II		93		85	93		dBc
@ –1 dBFS	15.5 MHz	25°C	II		92		85	92		dBc
	30.5 MHz	25°C	V		92			92		dBc
TWO-TONE SFDR[2, 3, 4]		Full	V		100			100		dBFS
TWO-TONE IMD REJECTION[2, 4]										
F1, F2 @ –7 dBFS		Full	V		90			90		dBc
ANALOG INPUT BANDWIDTH		25°C	V		250			250		MHz

NOTES
[1]All ac specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially.
[2]AV_{CC} = 5 V to 5.25 V for rated ac performance.
[3]Analog input signal power swept from –7 dBFS to –100 dBFS.
[4]F1 = 15 MHz, F2 = 15.5 MHz.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE and $\overline{ENCODE}$ = Maximum Conversion Rate MSPS; T_{MIN} = –25°C, T_{MAX} = +85°C, C_{LOAD} = 10 pF)

Parameter	Name	Temp	Test Level	AD6644AST-40/65 Min	AD6644AST-40/65 Typ	AD6644AST-40/65 Max	Unit
ENCODE INPUT PARAMETERS[1]							
Encode Period[1] @ 65 MSPS	t_{ENC}	Full	V		15.4		ns
Encode Period[1] @ 40 MSPS	t_{ENC}	Full	V		25		ns
Encode Pulsewidth High[2] @ 65 MSPS	t_{ENCH}	Full	IV	6.2	7.7	9.2	ns
Encode Pulsewidth Low @ 65 MSPS	t_{ENCL}	Full	IV	6.2	7.7	9.2	ns
ENCODE/DATA READY							
Encode Rising to Data Ready Falling	t_{DR}	Full	IV	2.6	3.4	4.6	ns
Encode Rising to Data Ready Rising	t_{E_DR}				$t_{ENCH} + t_{DR}$		
@ 65 MSPS (50% Duty Cycle)		Full	IV	10.3	11.1	12.3	ns
@ 40 MSPS (50% Duty Cycle)		Full	IV	15.1	15.9	17.1	ns
ENCODE/DATA (D13:0), OVR							
ENC to DATA Falling Low	t_{E_FL}	Full	IV	3.8	5.5	9.2	ns
ENC to DATA Rising Low	t_{E_RL}	Full	IV	3.0	4.3	6.4	ns
ENCODE to DATA Delay (Hold Time)[3]	t_{H_E}	Full	IV	3.0	4.3	6.4	ns
ENCODE to DATA Delay (Setup Time)[4]	t_{S_E}				$t_{ENC} - t_{E\_FL}$		
Encode = 65 MSPS (50% Duty Cycle)		Full	IV	6.2	9.8	11.6	ns
Encode = 40 MSPS (50% Duty Cycle)		Full	IV	15.9	19.4	21.2	ns

AD6644–SPECIFICATIONS

Parameter	Name	Temp	Test Level	AD6644AST-40/65 Min	Typ	Max	Unit
DATA READY (DRY[5])/DATA, OVR							
Data Ready to DATA Delay (Hold Time)[2]	t_{H_DR}				Note 6		
Encode = 65 MSPS (50% Duty Cycle)		Full	IV	8.0	8.6	9.4	ns
Encode = 40 MSPS (50% Duty Cycle)		Full	IV	12.8	13.4	14.2	ns
Data Ready to DATA Delay (Setup Time)[2]	t_{S_DR}				Note 6		
@ 65 MSPS (50% Duty Cycle)		Full	IV	3.2	5.5	6.5	ns
@ 40 MSPS (50% Duty Cycle)		Full	IV	8.0	10.3	11.3	ns
APERTURE DELAY	t_A	25°C	V		100		ps
APERTURE UNCERTAINTY (JITTER)	t_J	25°C	V		0.2		ps rms

NOTES

[1]Several timing parameters are a function of t_{ENC} and t_{ENCH}.

[2]To compensate for a change in duty cycle for t_{H_DR} and t_{S_DR} use the following equations:

$Newt_{H\_DR} = (t_{H\_DR} - \%\ Change(t_{ENCH})) \times t_{ENC}/2$

$Newt_{S\_DR} = (t_{S\_DR} - \%\ Change(t_{ENCH})) \times t_{ENC}/2$.

[3]ENCODE to DATA Delay (Hold Time) is the absolute minimum propagation delay through the analog-to-digital converter.

[4]ENCODE to DATA Delay (Setup Time) is calculated relative to 65 MSPS (50% duty cycle). In order to calculate t_{S_E} for a given encode use the following equation:

$Newt_{S\_E} = t_{ENC(NEW)} - t_{ENC} + t_{S\_E}$ (i.e., for 40 MSPS: $Newt_{S\_E(TYP)} = 25 \times 10^{-9} - 15.38 \times 10^{-9} + 9.8 \times 10^{-9} = 19.4 \times 10^{-9}$).

[5]DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock will correspondingly change the duty cycle of DRY.

[6]Data Ready to DATA Delay (t_{H_DR} and t_{S_DR}) is calculated relative to 65 MSPS (50% duty cycle) and is dependent on t_{ENC} and duty cycle. In order to calculate t_{H_DR} and t_{S_DR} for a given encode use the following equations:

$Newt_{H\_DR} = t_{ENC(NEW)}/2 - t_{ENCH} + t_{H\_DR}$ (i.e., for 40 MSPS: $Newt_{H\_DR(TYP)} = 12.5 \times 10^{-9} - 7.69 \times 10^{-9} + 8.6 \times 10^{-9} = 13.4 \times 10^{-9}$).

$Newt_{S\_DR} = t_{ENC(NEW)}/2 - t_{ENCH} + t_{S\_DR}$ (i.e., for 40 MSPS: $Newt_{S\_DR(TYP)} = 12.5 \times 10^{-9} - 7.69 \times 10^{-9} + 5.5 \times 10^{-9} = 10.3 \times 10^{-9}$).

Specifications subject to change without notice.

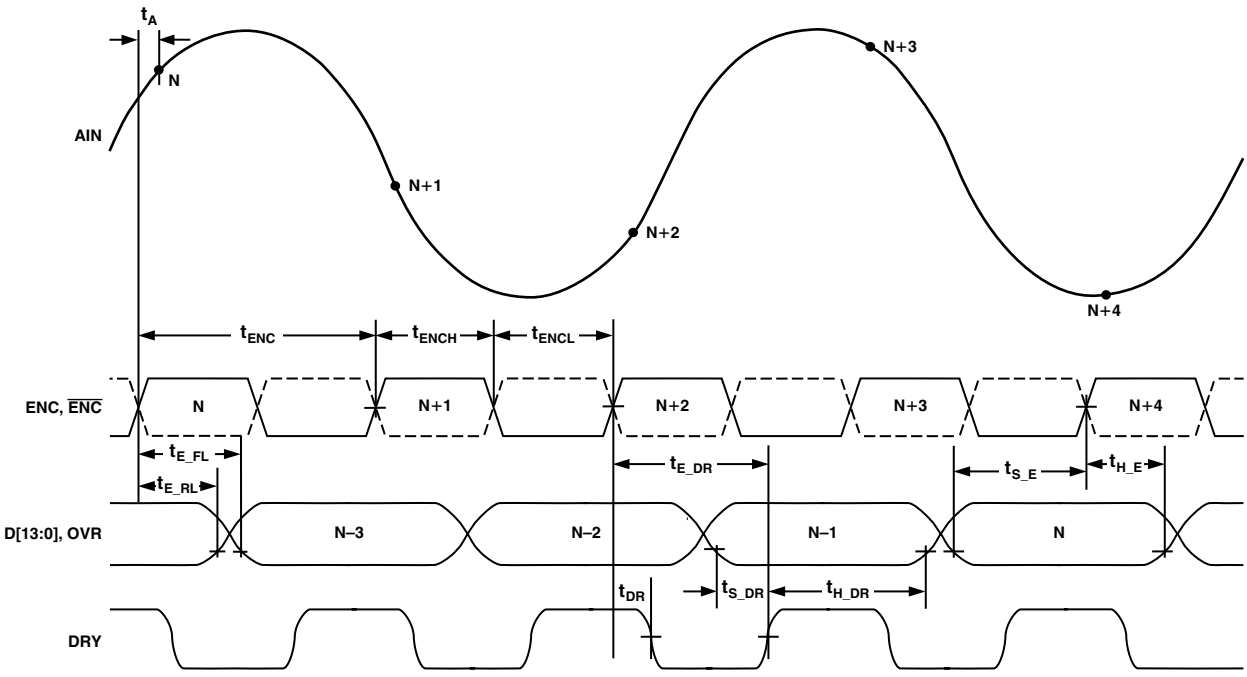


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Unit
ELECTRICAL			
AV_{CC} Voltage	0	7	V
DV_{CC} Voltage	0	7	V
Analog Input Voltage	0	AV_{CC}	V
Analog Input Current		25	mA
Digital Input Voltage	0	AV_{CC}	V
Digital Output Current		4	mA
ENVIRONMENTAL[2]			
Operating Temperature Range (Ambient)	–25	+85	°C
Maximum Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec)		300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (52-lead LQFP): θ_{JA} = 33°C/W; θ_{JC} = 11°C/W. These measurements were taken on a 6-layer board in still air with a solid ground plane.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at 25°C, and guaranteed by design and characterization at temperature extremes.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6644AST-40	–25°C to +85°C (Ambient)	52-Lead LQFP (Low Profile Quad Flat Package)	ST-52
AD6644AST-65	–25°C to +85°C (Ambient)	52-Lead LQFP (Low Profile Quad Flat Package)	ST-52
AD6644ST/PCB		Evaluation Board with AD6644AST–65	

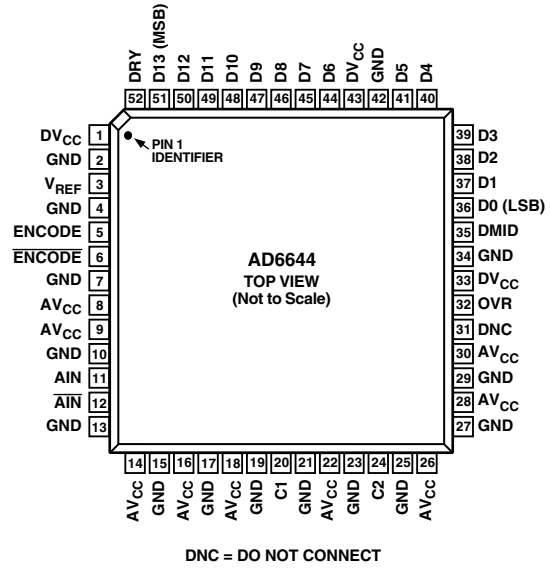
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6644 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 33, 43	DV_{CC}	3.3 V Power Supply (Digital) Output Stage Only.
2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	GND	Ground.
3	V_{REF}	2.4 V (Analog Reference). Bypass to ground with 0.1 µF microwave chip capacitor.
5	ENCODE	Encode Input; conversion initiated on rising edge.
6	$\overline{\text{ENCODE}}$	Complement of ENCODE; differential input.
8, 9, 14, 16, 18, 22, 26, 28, 30	AV_{CC}	5 V Analog Power Supply.
11	AIN	Analog Input.
12	$\overline{\text{AIN}}$	Complement of AIN; Differential Analog Input.
20	C1	Internal Voltage Reference; bypass to ground with 0.1 µF microwave chip capacitor.
24	C2	Internal Voltage Reference; bypass to ground with 0.1 µF microwave chip capacitor.
31	DNC	Do not connect this pin.
32	OVR	Overrange Bit; high indicates analog input exceeds ±FS.
35	DMID	Output Data Voltage Midpoint; approximately equal to $(DV_{CC})/2$.
36	D0 (LSB)	Digital Output Bit (Least Significant Bit); Twos Complement.
37–41, 44–50	D1–D5, D6–D12	Digital Output Bits in Twos Complement.
51	D13 (MSB)	Digital Output Bit (Most Significant Bit); Twos Complement.
52	DRY	Data Ready Output.

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input's phase 180° and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in the logic 1 state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in a low state. See text for timing implications of changing t_{ENCH}. At a given clock rate, these specs define an acceptable ENCODE duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{Full\ Scale} = 10\log\left[\frac{\frac{V^2_{Full\ Scale\ rms}}{|Z|_{Input}}}{0.001}\right]$$

Harmonic Distortion, 2nd
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, 3rd
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least-square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)

$$V_{NOISE} = \sqrt{|Z| \times 0.001 \times 10^{\left(\frac{FS_{dBm} - Signal_{dBFS}}{10}\right)}}$$

Where *Z* is the input impedance, *FS* is the full scale of the device for the frequency in question, *SNR* is the value for the particular input level and *Signal* is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the 2nd and 3rd harmonics) reported in dBc.

EQUIVALENT CIRCUITS

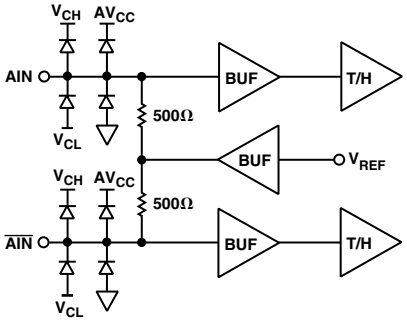


Figure 2. Analog Input Stage

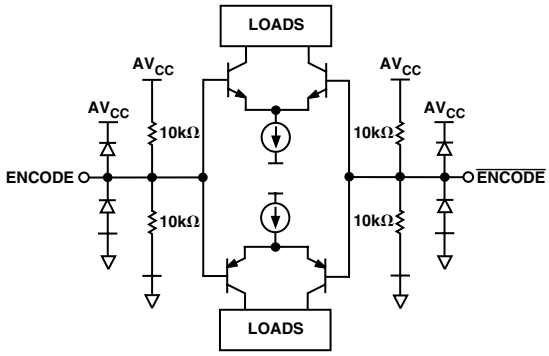


Figure 3. ENCODE Inputs

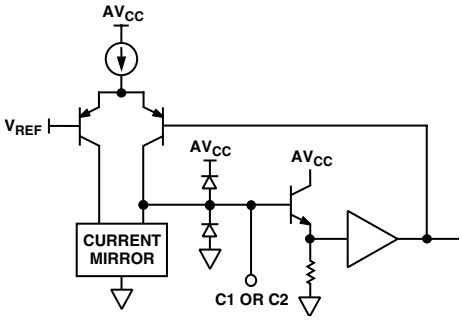


Figure 4. Compensation Pin, C1 or C2

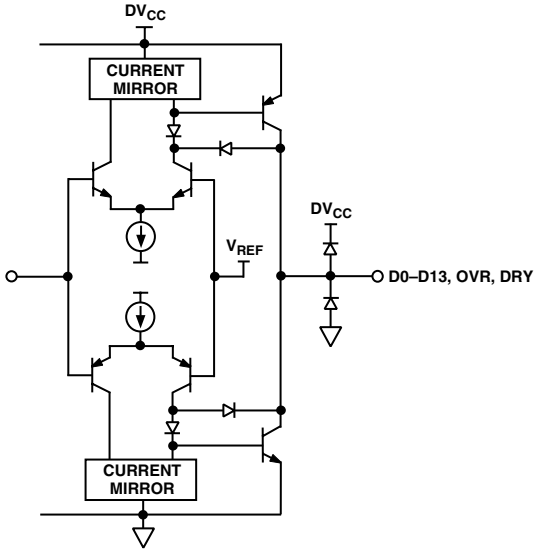


Figure 5. Digital Output Stage

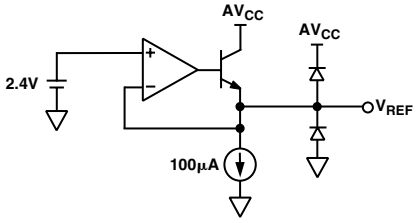


Figure 6. 2.4 V Reference

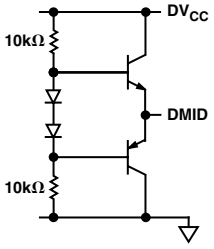
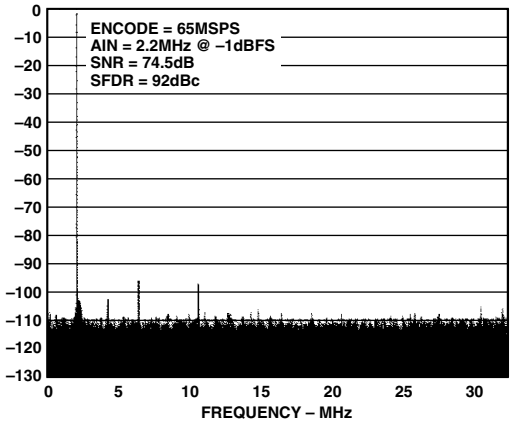
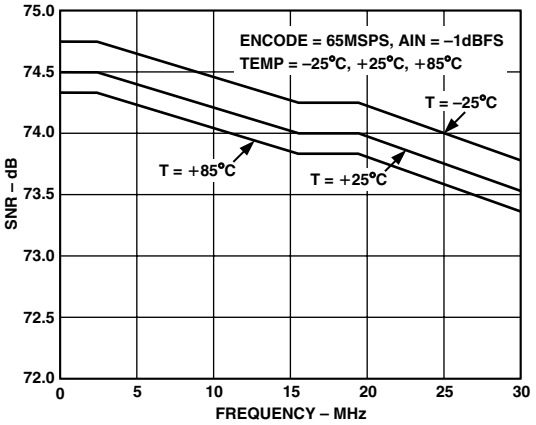


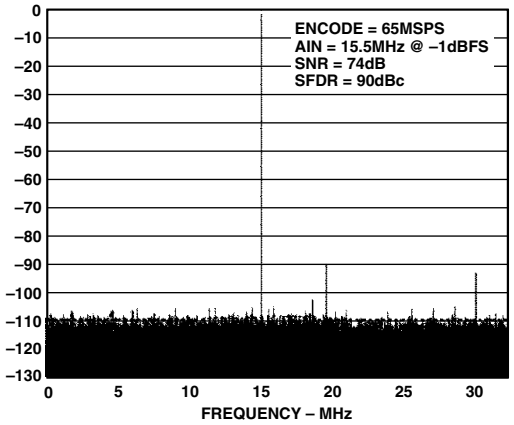
Figure 7. DMID Reference



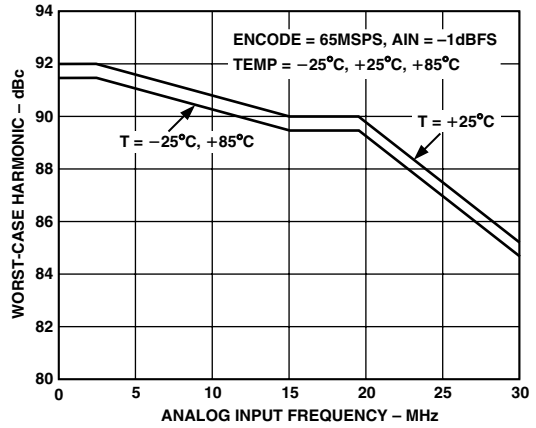
TPC 1. Single Tone at 2.2 MHz



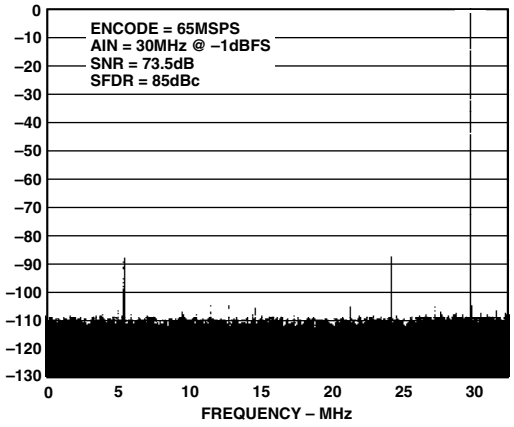
TPC 4. Noise vs. Analog Frequency (Nyquist)



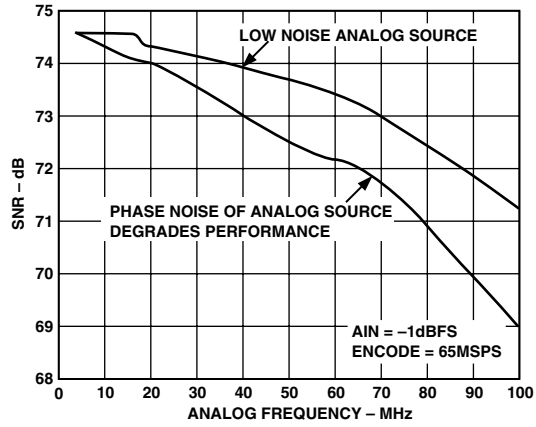
TPC 2. Single Tone at 15.5 MHz



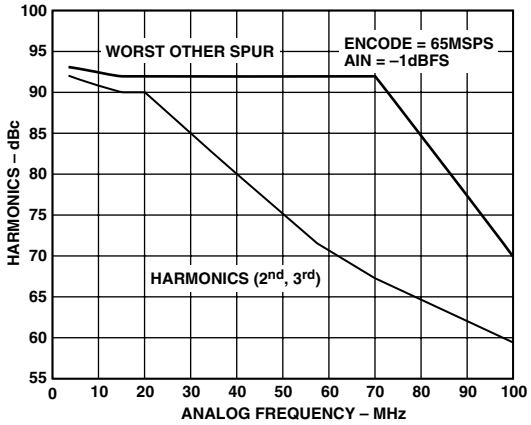
TPC 5. Harmonics vs. Analog Frequency (Nyquist)



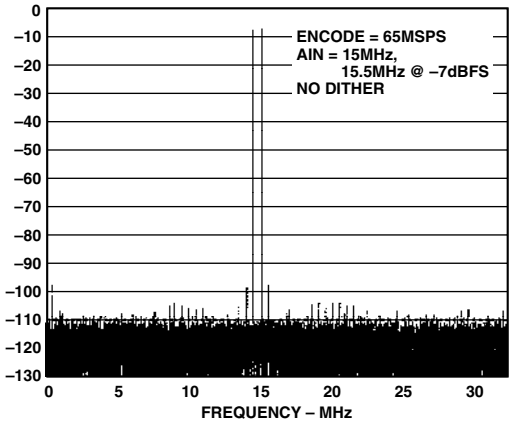
TPC 3. Single Tone at 30 MHz



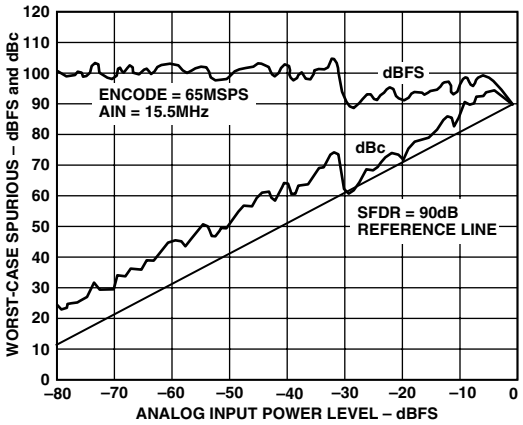
TPC 6. Noise vs. Analog Frequency (IF)



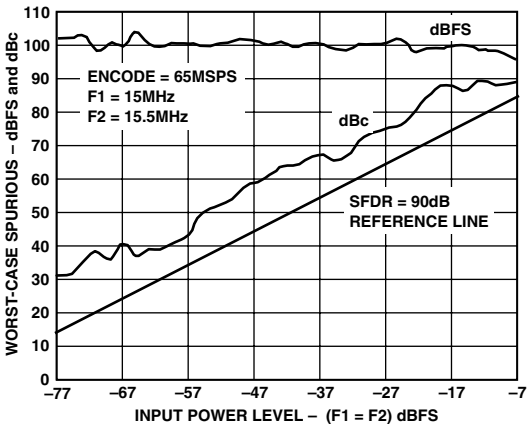
TPC 7. Harmonics vs. Analog Frequency (IF)



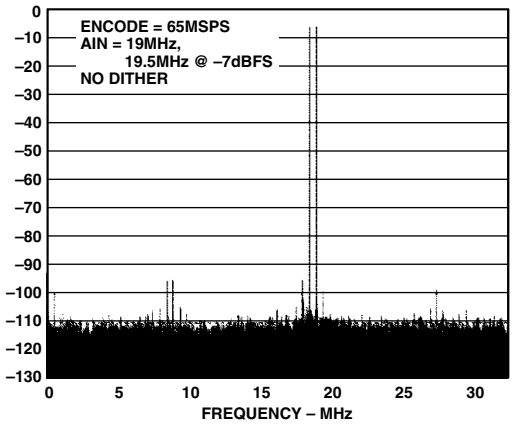
TPC 10. Two Tones at 15 MHz and 15.5 MHz



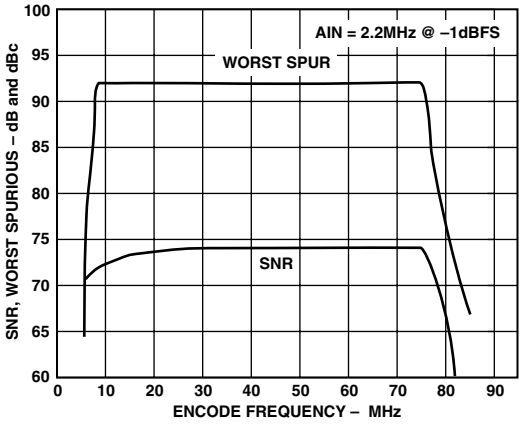
TPC 8. Single-Tone SFDR



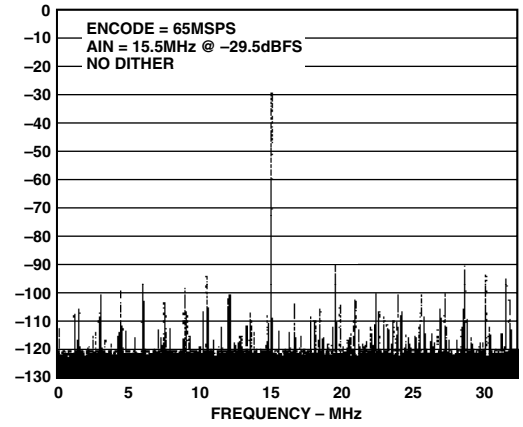
TPC 11. Two-Tone SFDR



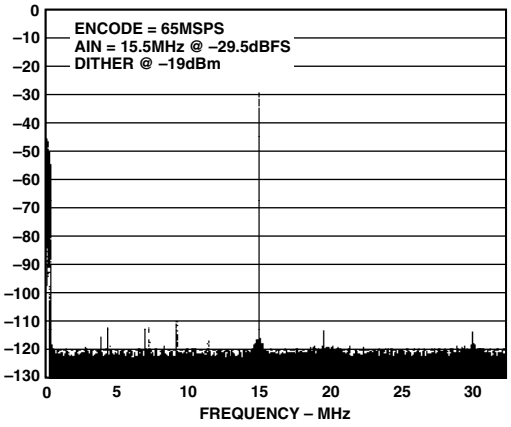
TPC 9. Two Tones at 19 MHz and 19.5 MHz



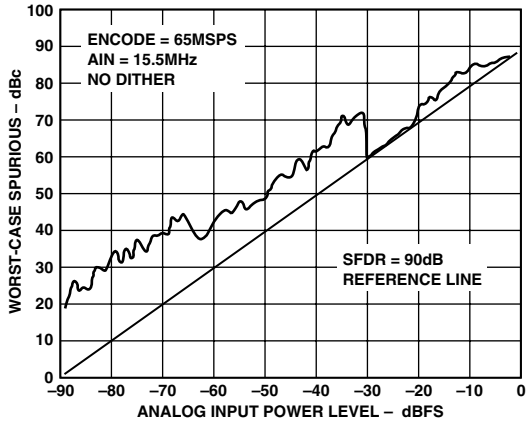
TPC 12. SNR, Worst Spurious vs. Encode



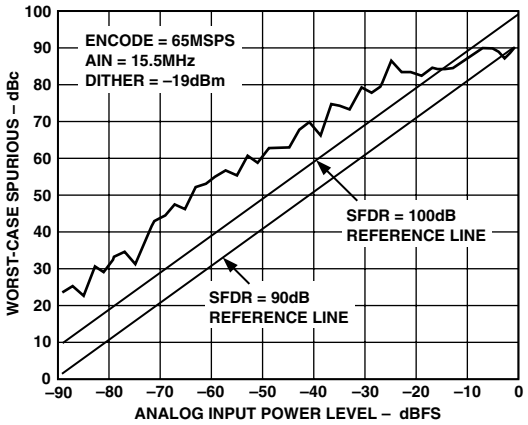
TPC 13. 1M FFT without Dither



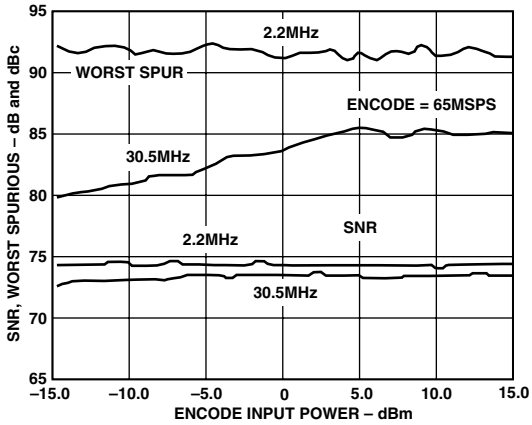
TPC 16. 1M FFT with Dither



TPC 14. SFDR without Dither



TPC 17. SFDR with Dither



TPC 15. SNR, Worst Spurious vs. Clamped Encode Power (See Figure 8)

THEORY OF OPERATION

The AD6644 analog-to-digital converter (ADC) employs a three stage subrange architecture. This design approach achieves the required accuracy and speed while maintaining low power and small die size.

As shown in the functional block diagram, the AD6644 has complementary analog input pins, AIN and $\overline{\text{AIN}}$. Each analog input is centered at 2.4 V and should swing ±0.55 V around this reference (Figure 2). Since AIN and $\overline{\text{AIN}}$ are 180° out of phase, the differential analog input signal is 2.2 V peak-to-peak.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives a 5-bit digital-to-analog converter, DAC1. DAC1 requires 14 bits of precision, which is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residue signal is applied to a second conversion stage consisting of a 5-bit ADC2, 5-bit DAC2, and pipeline TH4. The second DAC requires 10 bits of precision, which is met by the process with no trim. The input to TH5 is a second residue signal generated by subtracting the quantized output of DAC2 from the first residue signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS compatible word, coded as twos complement.

APPLYING THE AD6644

Encoding the AD6644

The AD6644 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 70 MHz input signals when using a high jitter clock source. See Analog Devices' Application Note AN-501, "Aperture Uncertainty and ADC System Performance," for complete details.

For optimum performance, the AD6644 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Shown below is one preferred method for clocking the AD6644. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6644 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD6644, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100 Ω) is placed in series with the primary.

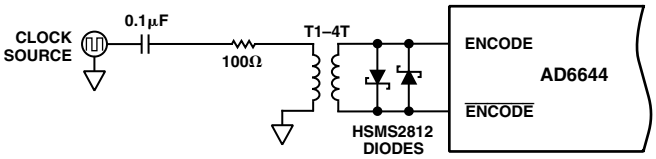


Figure 8. Crystal Clock Oscillator – Differential Encode

If a low jitter ECL/PECL clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown below. A device that offers excellent jitter performance is the MC100LVEL16 (or same family) from Motorola.

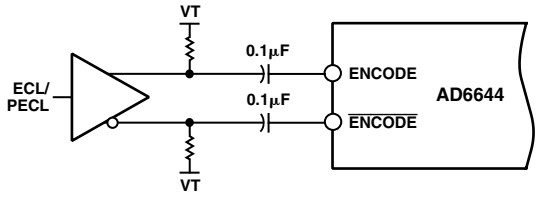


Figure 9. Differential ECL for Encode

Analog Input

As with most new high speed, high dynamic range analog-to-digital converters, the analog input to the AD6644 is differential. Differential inputs allow much improvement in performance on-chip as signals are processed through the analog stages. Most of the improvement is a result of differential analog stages having high rejection of even order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection of stray signals such as ground and power noise. Also, they provide good rejection of common-mode signals such as local oscillator feedthrough.

The AD6644 input voltage range is offset from ground by 2.4 V. Each analog input connects through a 500 Ω resistor to a 2.4 V bias voltage and to the input of a differential buffer (Figure 2). The resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6644 should be ac-coupled to the input pins. Since the differential input impedance of the AD6644 is 1 kΩ, the analog input power requirement is only –2 dBm, simplifying the driver amplifier in many cases. To take full advantage of this high input impedance, a 20:1 transformer would be required. This is a large ratio and could result in unsatisfactory performance. In this case, a lower step-up ratio could be used. The recommended method for driving the analog input of the AD6644 is to use a 4:1 RF transformer. For example, if R_T were set to 60.4 Ω and R_S were set to 25 Ω, along with a 4:1 transformer, the input would match to a 50 Ω source with a full-scale drive of 4.8 dBm. Series resistors (R_S) on the secondary side of the transformer should be used to isolate the transformer from the A/D. This will limit the amount of dynamic current from the A/D flowing back into the secondary of the transformer. The terminating resistor (R_T) should be placed on the primary side of the transformer.

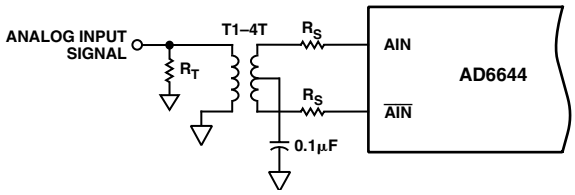


Figure 10. Transformer-Coupled Analog Input Circuit

In applications where dc-coupling is required, a new differential output op amp from Analog Devices, the AD8138, can be used to drive the AD6644 (Figure 11). The AD8138 op amp provides single-ended-to-differential conversion, which reduces overall system cost and minimizes layout requirements.

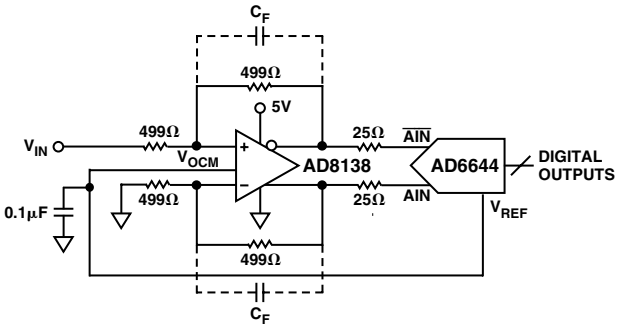


Figure 11. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be "received" by the AD6644. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 μF chip capacitors.

The AD6644 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC}. AV_{CC} and DV_{CC} should be separate power supplies. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD6644 is specified for DV_{CC} = 3.3 V as this is a common supply for digital ASICs.

Output Loading

Care must be taken when designing the data receivers for the AD6644. It is recommended that the digital outputs drive a series resistor (e.g., 100 Ω) followed by a gate like the 74LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic of Figure 13. The digital outputs of the AD6644 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace will have a load of approximately 10 pF. Therefore, as each bit switches, 10 mA (10 pF × 1 V ÷ 1 ns) of dynamic current per bit will flow in or out of the device. A full scale transition can cause up to 140 mA (14 bits × 10 mA/bit) of current to flow through the output stages. The series resistors should be placed as close to the AD6644 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD6644. It should also be noted that extra capacitive loading will increase output timing and invalidate timing specifications. Digital output timing is guaranteed with 10 pF loads.

Layout Information

The schematic of the evaluation board (Figure 13) represents a typical implementation of the AD6644. A multilayer board is recommended to achieve the best results. It is highly recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6644 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6644, minimal capacitive loading should be placed on these outputs. It is recommended that a fan-out of only one gate be used for all AD6644 digital outputs.

The layout of the encode circuit is equally critical. Any noise received on this circuitry will result in corruption in the digitization process and lower overall performance. The Encode clock must be isolated from the digital outputs and the analog inputs.

Jitter Considerations

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, Equation 1 accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = -20 \times \log\left[\left[\frac{(1+\varepsilon)}{2^N}\right]^2 + (2 \times \pi \times f_{ANALOG} \times t_{J\ RMS})^2 + \left(\frac{V_{NOISE\ RMS}}{2^N}\right)^2\right]^{1/2} \quad (1)$$

f_{ANALOG} = analog input frequency.

$t_{J\ RMS}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry).

ε = average DNL of the ADC (typically 0.41 LSB).

N = Number of bits in the ADC.

$V_{NOISE\ RMS}$ = V rms thermal noise referred to the analog input of the ADC (typically 2.5 LSB).

For a 14-bit analog-to-digital converter like the AD6644, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrates the expected SNR performance of the AD6644 as jitter increases. The chart is derived from the above equation.

For a complete discussion of aperture jitter, consult Analog Devices' Application Note AN-501, "Aperture Uncertainty and ADC System Performance."

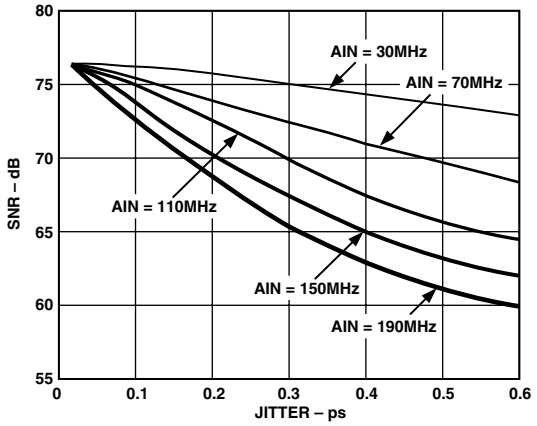


Figure 12. SNR vs. Jitter

EVALUATION BOARD

The evaluation board for the AD6644 is straightforward, containing all required circuitry for evaluating the device. The only external connections required are power supplies, clock, and the analog inputs. The evaluation board includes the option for an on-board clock oscillator for ENCODE.

Power to the analog supply pins of the AD6644 is connected via the power terminal block (PCTB2). Power for the digital interface is supplied via Pin 1 of J6. The J2 connector mates directly with SoftCell Receive Signal Processor (AD6620, AD6624) evaluation boards, allowing complete evaluation of system performance.

The analog input is connected via a BNC connector, AIN, which is transformer-coupled to the AD6644 inputs. The transformer has a turns ratio of 1:4 to reduce the amount of input power required to drive the AD6644.

The encode signal may be generated using an on-board crystal oscillator, U5. The on-board oscillator may be replaced by an external encode source via the SMA connector labeled OPT_CLK or BNC connector labeled ENCODE. If an external source is used, it must be a high quality and very low phase noise source.

The AD6644 output data is latched using 74LCX574 (U7, U2) latches. The clock for these latches is determined by selecting jumper E3–E4 or E4–E5. E3 to E5 is a just a gate delayed version of the clock, while connecting E4 to E5 utilizes the Data Ready of the AD6644 to latch the output data. A clock is also distributed with the output data (J2) that is labeled BUFLAT (Pins 19 and 20, J2).

AD6644ST/PCB Bill of Material

Item	Quantity	Reference	Description
1	2	C1, C2	Tantalum Chip Capacitor 10 µF
2	19	C3, C4, C7, C8, C9, C10, C11, C16, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31,C32,	Ceramic Chip Capacitor 0508, 0.1 µF
3	8	C12, C13, C14, C17, C18, C19, C20, C21	Ceramic Chip Capacitor 0508, 0.01 µF
4	1	CR1	HSMS2812 Surface Mount Diode
5	1	E3, E4, E5	3-Pin Header
6	4	F1, F2, F3, F4	Ferrite (Optional)
7	2	J1, J6	PCTB2
8	1	J2	50-Pin Double Row Header
9	1	J3	SMA Connector
10	2	J4, J5	BNC Connector
11	1	R1	Surface-Mount Resistor 1206, 100 Ω
12	1	R2	Surface-Mount Resistor 1206, 60.4 Ω
13	4	R3, R4, R5, R8	Surface-Mount Resistor 0805, 499 Ω (Optional, DC-Coupling Only)
14	2	R6, R7	Surface-Mount Resistor 0805, 25 Ω
15	1	R9	Surface-Mount Resistor 0805, 348 Ω
16	1	R10	Surface-Mount Resistor 0805, 615 Ω
17	1	R35	Surface-Mount Resistor 0805, 49.9 Ω
18	30	R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65	Surface-Mount Resistor 0402, 100 Ω
19	2	T2, T3	Surface-Mount Transformer Mini-Circuits T4–1, 1:4 Ratio
20	1	U1	AD6644AST 14-Bit 65 MSPS A/D Converter
21	2	U2, U7	74LCX574 Octal Latch
22	1	U3	AD8138 Single-to-Differential Amplifier (Optional, DC Coupling Only)
23	2	U4, U6	NC7SZ32 Two Input OR Gate
24	1	U5	CTS Reeves Full-Size MX045 Crystal Clock Oscillator

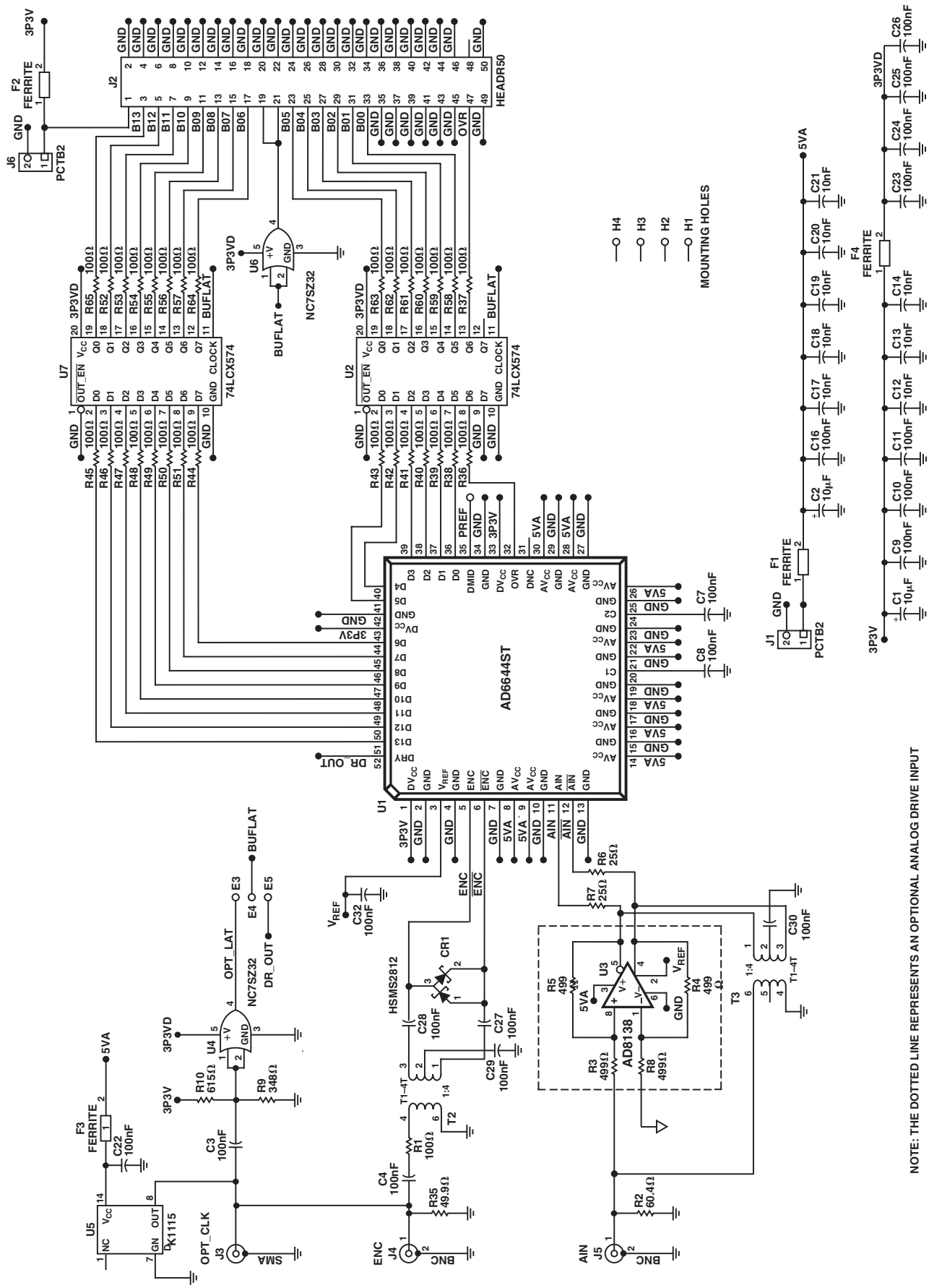


Figure 13. AD6644ST/PCB Schematic (GS02357D Schematic)

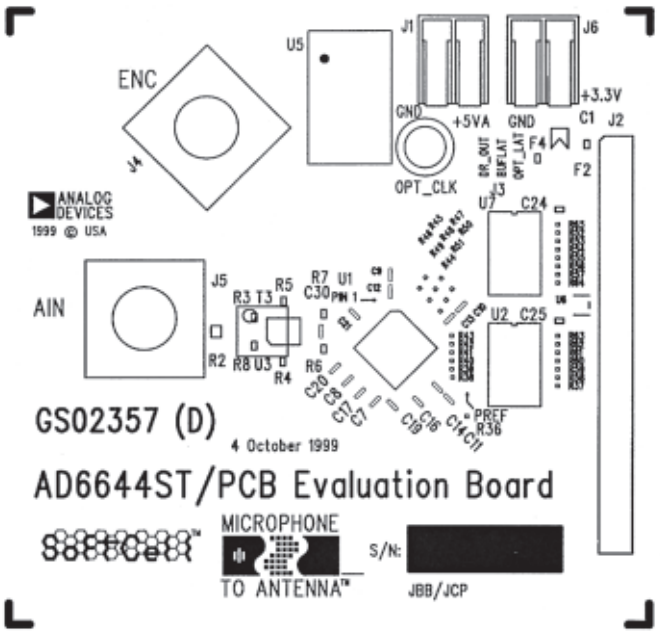


Figure 14. AD6644ST/PCB Top Side Silkscreen

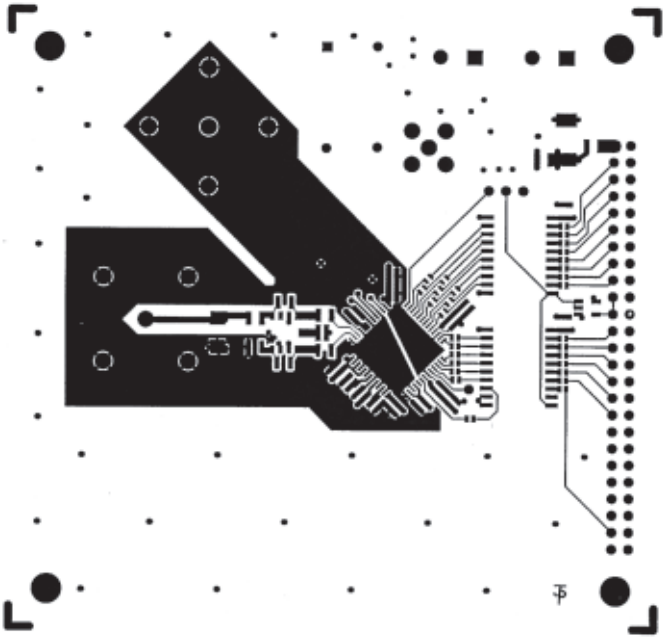


Figure 15. AD6644ST/PCB Top Side Copper

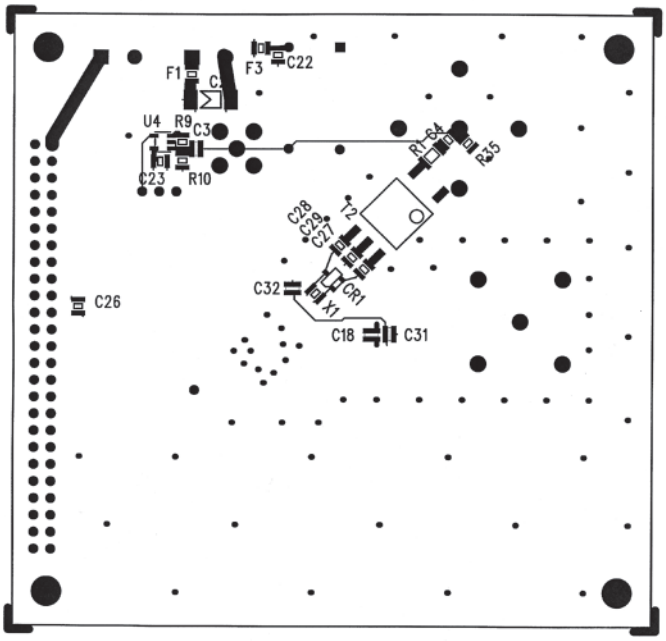


Figure 16. AD6644ST/PCB Bottom Side Silkscreen

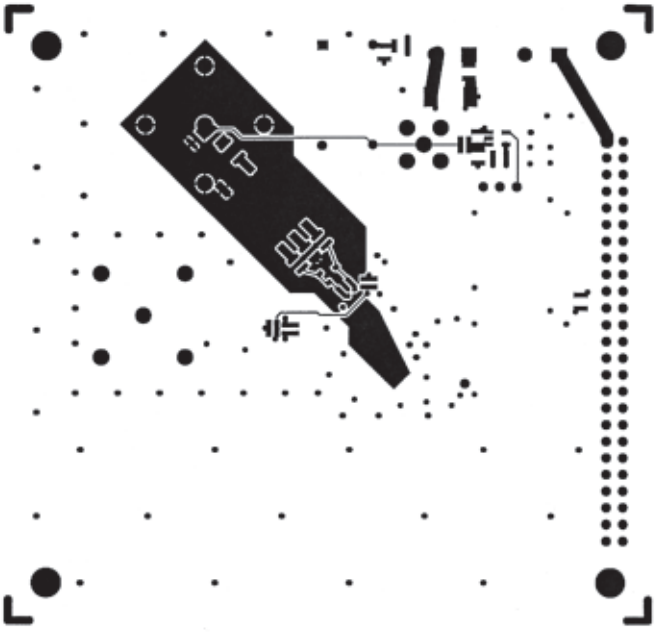


Figure 17. AD6644ST/PCB Bottom Side Copper

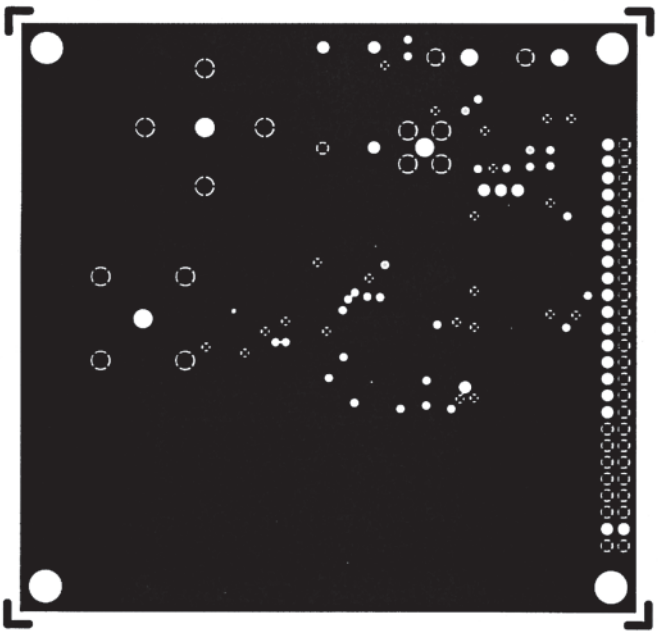


Figure 18. AD6644ST/PCB Ground Layer – Layers 2 and 5 (Negative)

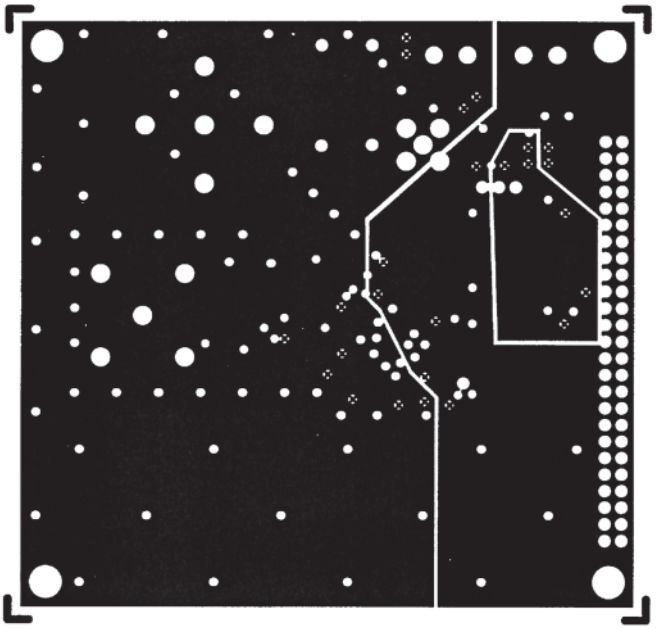
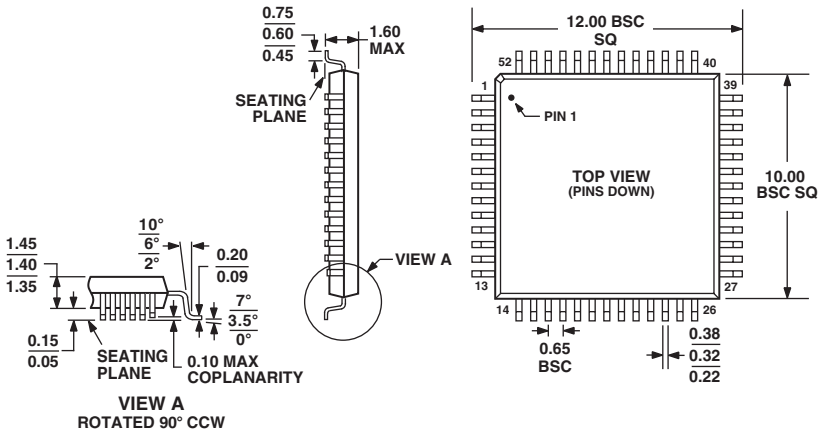


Figure 19. AD6644ST/PCB "Split" Power Layer – Layers 3 and 4 (Negative)

OUTLINE DIMENSIONS

52-Lead Low Profile Quad Flat Package [LQFP]
(ST-52)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BCC

Revision History

Location	Page
5/03—Data Sheet changed from REV. B to REV. C.	
Updated OUTLINE DIMENSIONS	19
3/03—Data Sheet changed from REV. A to REV. B.	
Change to DIGITAL SPECIFICATIONS Notes	2
3/03—Data Sheet changed from REV. 0 to REV. A.	
Edits to SPECIFICATIONS	2
Renumbering of Figures and TPCs	Universal
Updated OUTLINE DIMENSIONS	19

C00971–0–5/03(C)